

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	Divakaruni et al.	Conf. No.:	1387
Serial No.:	10/707,388	Art Unit:	2891
Filed:	12/10/2003	Examiner:	Fulk, Steven J.
Title:	SILICIDE RESISTOR IN BEOL LAYER OF SEMICONDUCTOR DEVICE AND METHOD	Docket No.:	FIS920030274US1 (IBMF-0032)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
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BRIEF OF APPELLANT

This is an appeal from the Final Rejection (Office Action) dated April, 11, 2008, rejecting claims 12-20. The requisite fee set forth in 37 C.F.R. §1.17 (c) was submitted on July 8, 2008.

REAL PARTY IN INTEREST

International Business Machines Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There is no related appeal or interference.

STATUS OF CLAIMS

As filed, this case included claims 1-20. Claims 12-18 and 20 remain pending, stand rejected, and form the basis of this appeal. Claims 1-11 and 19 have been cancelled. No claim has been allowed. The rejections of claims 12-18 and 20 are being appealed.

STATUS OF AMENDMENTS

No after-final amendment of claims was proposed following the Final Rejection of April 11, 2008.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention, as defined by independent claim 12, includes a resistor for a semiconductor device, the resistor comprising a silicide section positioned in a trough in one of a plurality of back-end-of-line (BEOL) layers (paragraphs [0017]-[0019], Fig. 8). A polysilicon is base positioned in the trough and below the silicide section (paragraph [0020]). The silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers (paragraph [0019]).

The present invention, as defined by independent claim 20, includes a semiconductor device comprising a silicide resistor in one of a plurality of back-end-of-line (BEOL) layers (paragraphs [0017]-[0019], Fig. 8), the silicide resistor including a silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers (paragraph [0019]). A polysilicon base is positioned below the silicide section (paragraph

[0020]). The silicide section and the polysilicon base are positioned in a trough in one of the plurality of back-end-of-line (BEOL) layers (paragraph [0023] and Figure 8).

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 12-18 and 20 are indefinite under 35 USC §112, second paragraph.
2. Whether claims 12, 18 and 20 are anticipated under 35 U.S.C. §102(b) by Yoo et al. (US 6,168,984), hereinafter “Yoo”.
3. Whether claims 13-17 are obvious under 35 U.S.C. §103(a) by Yoo in view of Wolf (Wolf, *Silicon Processing for the VLSI Era*, 1990, Volume II, pp 146, 176, 193) hereinafter “Wolf.”.

ARGUMENTS

1. Claims 12-18 are not indefinite under 35 USC §112, second paragraph.

The Office takes issue with the claim language “a silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers”. Specifically, the Office imports the limitation “probable” into claims 12 and 20. (Final Office Action of April 11, 2008 paragraph 2). Appellants assert this is not permissible. *Altiris Inc. v. Symantec Corp.*, 318 F.3d 1363, 1371, 65 USPQ2d 1865, 1869-70 (Fed. Cir. 2003). The claim language specifically states “wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers”. This language on its face is clear to the skilled

artisan as a silicidation temperature less than a damaging temperature and BEOL layers are all clear to a person of ordinary skill in the art.

The Office contends that; “Because the specification does not establish a probability of damage at the silicidation temperature, it is not sufficiently clear whether or not damage occurs to the BEOL layers”. It is important not to import into a claim limitations that are not part of the claim. (MPEP 2.111.1 (II)). This is what the Office is doing. Appellant has provided an invention that allows a passive resistor to be processed without high temperature anneals that would damage other BEOL wiring structures [paragraph 0004]. The BEOL layers can be of various materials [paragraph 0021] and the silicidation temperature is dependent on the silicide [paragraph 0020]. Thus, a damaging temperature to the BEOL layers depends on certain factors that are known to the skilled artisan. Either the BEOL wiring layers are damaged when processed or they or not, and this determination can be made without undue experimentation through a test of the BEOL layers after processing. In view of the foregoing, Applicants respectfully request withdrawal of the rejection under 35 USC §112, second paragraph.

2. Claims 12, 18 and 20 are not anticipated Yoo.

The Office asserts that Yoo discloses a silicide resistor formed of a poly-silicon layer and a tungsten silicide layer. The Examiner asserts that the structure referenced in Figure 13 of Yoo has an inherent resistance and thus considered a resistor in one of a plurality of BEOL layers (formed from an interlayer dielectric over FEOL layers 1-17, layer 31 is a second BEOL layer, thus 27 and 31 are a plurality), the silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers. This argument ignores the teaching of

Yoo. The structure referred to in Yoo is a bitline structure (col. 8 lines 65-66) in an opening (col. 8, lines 48-51). Thus, the characterization that Yoo teaches a silicide resistor in a trough is faulty. A trough is defined as a channel. The opening in Yoo is not a channel as it extends through layer 27. Thus, Yoo does not show a trough, an element of the claimed invention and the anticipation rejection is improper.

Moreover a bitline is not a resistor and a bitline structure positioned in an opening that connects each side of insulating layer 27 is not a resistor positioned in a trough. A bit-line is an electrical connection. Therefore, Yoo teaches that the silicide section is in actuality an electrical connector. This teaching in Yoo is contrary to Appellants teaching that the silicide section functions as a resistor. This is further evidence that Yoo does not anticipate the present invention.

3. Claims 13-17 are not rendered obvious by Yoo in view of Wolf.

With respect to claims 13-17 Wolf is cited for teaching group VII silicides. Such disclosures of the silicides substituted into the structure of Yoo would not produce Appellants invention. There would not be a silicide resistor in a trough as claimed but a bitline in an opening for use in a DRAM semiconductor device. In addition, both Wolf references only disclose using the silicide materials for interconnect applications, not for a resistor application as claimed in the current invention. Thus, like Yoo above, Wolf teaches away from the present invention as claimed. The combination proposed could not produce a silicide resistor in a trough. Therefore a combination of the references does not provide a *prima facie* obviousness-type rejection.

Appellants respectfully submit that the application is in condition for allowance. Should the Examiner believe that anything further is necessary to place the application in better condition for allowance, the Examiner is requested to contact Appellants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

/Carl F. Ruoff/

Date: September 8, 2008

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CLAIMS APPENDIX

12. A resistor for a semiconductor device, the resistor comprising:
a silicide section positioned in a trough in one of a plurality of back-end-of-line (BEOL) layers; and
a polysilicon base positioned in the trough and below the silicide section;
wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers.
13. The resistor of claim 12, wherein the silicide section includes cobalt silicide (CoSi) and has a resistivity of no less than approximately $14\ \mu$ -ohms/cm and no greater than approximately $20\ \mu$ -ohms/cm.
14. The resistor of claim 12, wherein the silicide section includes palladium silicide (PdSi) and has a resistivity of no less than approximately $25\ \mu$ -ohms/cm and no greater than approximately $30\ \mu$ -ohms/cm.
15. The resistor of claim 12, wherein the silicide section includes platinum silicide (PtSi) and has a resistivity of no less than approximately $26\ \mu$ -ohms/cm and no greater than approximately $35\ \mu$ -ohms/cm.

16. The resistor of claim 12, wherein the silicide section includes nickel silicide (NiSi) and has a resistivity of no less than approximately $14\ \mu$ -ohms/cm and no greater than approximately $20\ \mu$ -ohms/cm.

17. The resistor of claim 12, wherein the silicide section includes di-nickel silicide (Ni_2Si) and has a resistivity of no less than approximately $35\ \mu$ -ohms/cm and no greater than approximately $50\ \mu$ -ohms/cm.

18. The resistor of claim 12, wherein the silicide section includes one of molybdenum silicide (MoSi_2) and tungsten silicide (WSi_2).

20. A semiconductor device comprising:

a silicide resistor in one of a plurality of back-end-of-line (BEOL) layers, the silicide resistor including a silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers and a polysilicon base positioned below the silicide section;

wherein the silicide section and the polysilicon base are positioned in a trough in one of the plurality of back-end-of-line (BEOL) layers.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

There is no related proceeding.